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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/905,633	07/13/2001	Kelly T. Hurley	2000-0100.00	3692

7590

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EXAMINER

NGUYEN, KHIEM D

ART UNIT

PAPER NUMBER

2823

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/905,633

Applicant(s)

HURLEY, KELLY T.

Examiner

Khiem D Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) 11-19 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 July 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election without traverse of claims 1-10 in Paper No. 3 is acknowledged.

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 3 is rejected under 35 U.S.C. 102(b) as being anticipated by Kamitani (U.S. Patent 6,188,115).

Kamitani teaches a method for forming a flash memory device on a semiconductor assembly comprising forming a metal interconnect 15 running a major length of a series of source electrodes 43 connected together by a conductively doped active are, said source electrodes formed in a self-aligning manner to their respective gate electrodes, said metal interconnect having a majority of a bottom surface making contact to said conductively doped active area (See col. 9, lines 4 to 42 and FIG. 17).

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2 and 4-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamitani (U.S. Patent 6,188,115) in view of Watanabe et al. (IEDM, 98 pp. 975-978).

Kamitani teaches a method for forming a flash memory device in a semiconductor assembly, comprising the steps of (See col. 9, lines 4 to 42 and FIG. 17):

forming a series of floating gate devices 4 having their source electrodes 43 connected together by a conductive implant into a defined active area, each source electrode being self-aligned to a respective gate electrode.

forming a metal interconnect 15 running a major length of said connected together source electrodes, said metal interconnect making a substantially continuous contact therebetween; and,

forming a metal drain plug 15 for each floating gate device of said series of floating gate devices, said metal drain plug self-aligned to and connected between a drain electrode 12 of each said floating gate device 4 and a digit line 72.

Kamitani fails to teach forming a nitride barrier layer overlying each transistor gate and a planarized insulation layer over the nitride barrier layer then removing portions of the planarized insulation layer while using the nitride barrier layer to self-align an interconnect via to said source electrodes and wherein the interconnect and drain plug comprises tungsten-base (W) as recited in present claims 4 and 7-10.

Watanabe teaches forming a nitride barrier layer overlying each transistor gate and a planarized insulation layer over the nitride barrier layer then removing portions of the planarized insulation layer while using the nitride barrier layer to self-align an interconnect via to the source electrodes and wherein the interconnect comprise tungsten-

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base (W) (See pp. 975-976 and FIG. 1 (a)-(b)). It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Watanabe's teaching into Kamitani's method because in doing so a high density flash memory can be obtained (See the Abstract).


### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaudhuri Olik can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-9179 for regular communications and (703) 746-9179 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.  
November 15, 2002

  
Olik Chaudhuri  
Supervisory Patent Examiner  
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